Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**BASE**

**EMITTER**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: Base = .0041” X .0043” Emitter = .0061” X .004”**

**Backside Potential: Collector**

**Mask Ref: 12**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 10/4/21**

**MFG: FAIRCHILD THICKNESS .007” P/N: 2N3053**

**DG 10.1.2**

#### Rev B, 7/19/02